

When the signal WSTRESSB is in a first (normal) state, the circuit 106 may be configured to present, in one example, a digital complement of the signal EXT_WEB as the signal INT_WE. Alternatively, the signal EXT_WEB may be presented as the signal INT_WE. When the signal WSTRESSB is in a second (test) state, the circuit 106 may be configured to present the signal INT_WE with a predetermined pulse width in response to an edge of the signal EXT_WEB. The circuit 106 may be implemented with a number of delay elements. The delay elements may be programmed either electrically or by fuses. However, other types of programming may be implemented to meet the design criteria of a particular application. The delay elements may be used to program the predetermined pulse width of the signal INT_WE. The signal INT_WE may be a self-timed write stress test signal that may be used to predict cell failures.

Please replace the paragraph beginning at page 8, line 12 with the following paragraph:

Referring to FIG. 4, a block diagram illustrating an implementation of a circuit 106 for generating a self-timed write test signal in accordance with the present invention is shown. The circuit 106 may comprise, in one example, a gate 140 and a delay circuit (or block) 142. The gate 140 may be implemented in one

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example as a NOR gate. However, other types of gates may be implemented to meet the design criteria of a particular application. The signal EXT_WEB may be presented to a first input of the gate 140 and an input of the delay circuit 142. The delay circuit 142 may have an output that may present a signal to a second input of the gate 140. The signal INT_WE may be presented at an output of the gate 140.

Please replace the Abstract with the following paragraph:

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An integrated circuit includes a test circuit that may be configured to generate a test signal having a predetermined pulse width in response to a control input. The test signal may track process corners of the integrated circuit and may be used to predict a failure of the integrated circuit.
